

# Kawasaki USB2.0 Transceiver LSI & HS\_SIE Information Sheet

Preliminary rev 0.3c 2000.12

Note that this brochure is just preliminary description about the products. Kawasaki Steel Corporation and Kawasaki LSI does not assure its functionality nor feature and reserves the right to change them without notice.

## 1. General Description of KL5KUSB200ACFP

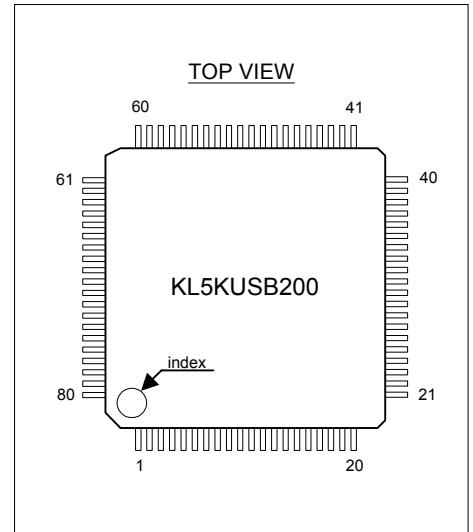
Kawasaki's KL5KUSB200 LSI is designed for USB2.0 high-speed capable transceiver based on USB2.0 Specification version 2.0. With external HS\_SIE, USB200 performs the excellent USB Bulk IN, Bulk OUT and interrupt transaction at 480 Mb/s extra high-speed.

Major chip functionality is as follows.

1. Capable of HS chirp generation and detection
2. Both High Speed (480Mb/s) and Full Speed (12Mb/s) supported
3. For incoming packet, phase locked, buffered, SYNC detected, NRZI decoded, bit unstuffed, CRC checked (optional), parallelized and transferred to SIE 16bit bus.
4. For outgoing packet, receive parallel data from SIE 16bit bus, serialized, CRC attached (optional), bit stuffed, NRZI encoded, SYNC and EOP attached and transferred to USB
5. USB bus status monitored, USB200 operation controlled by external HS\_SIE
6. Fully controlled by external signals.
7. UTMI function covered & stand-alone test mode supported.

With using as ASCP IP, we can offer you more flexible USB solution.

## 2. LQFP80 Package Outline



## 3. Product Feature

### Chip Feature

1. 0.35um stdcell technology (KS4000)
2. Analog Front End and digital logic co-design
3. External clock 48.0000MHz +/- 15 ppm
4. SIE 16bit synchronous bus with 30MHz CKOUT
5. operation voltage 3.3V ± 0.3 V
6. ambient temperature 0~70 C
7. device current (typical)
 

During operation	300mA (HS), 150mA (FS)
Suspended	100uA
8. LQFP80 package (12mm-sq)

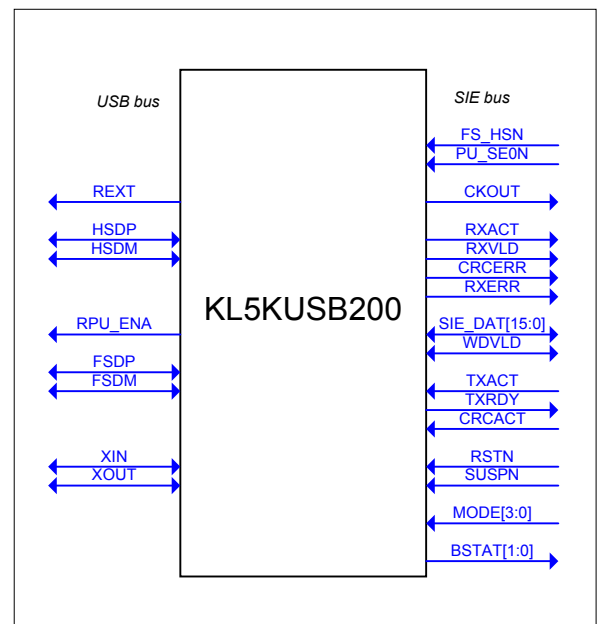
### External resistors

1. Rpu (1.5k ohm +/- 5%) as D+ pull-up resistor
2. Rs (39 ohm +/- 2%) as D+/D- FS driver series resistor

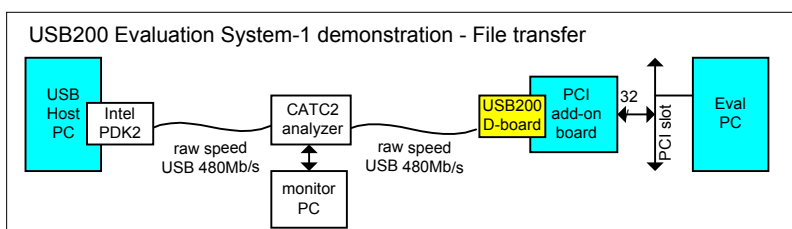
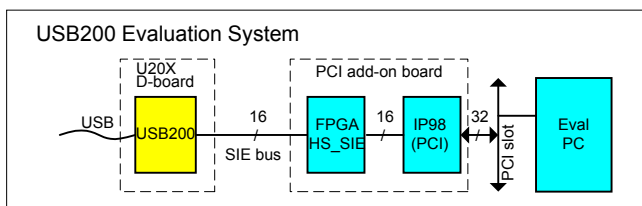
### Evaluation Package

1. U20X D-board -- USB200, Xtal, Rpu, Rps, USB B-connector
2. PCI add-on board -- ALTERA, IP98 (PCI IF)
3. HS\_SIE in ALTERA ROM
4. Software Example (PCI driver & Appli for eval PC and USB driver& Appli for USB host PC )

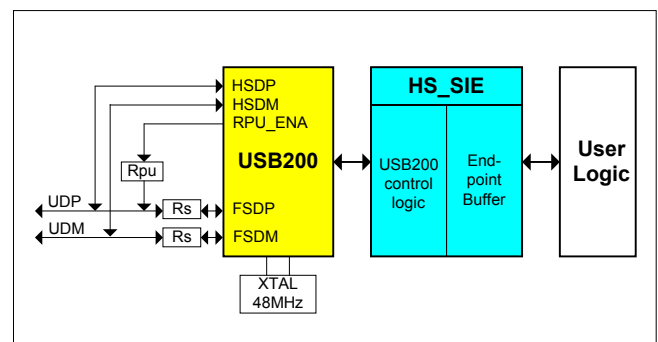
## 4. Logical Pin out



## 5. Evaluation System Overview



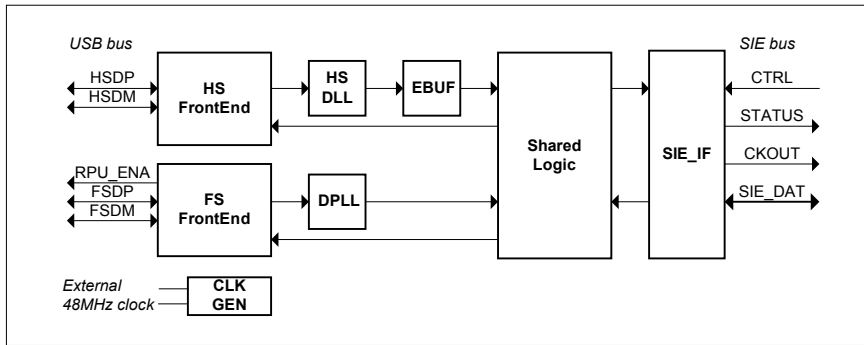
## 6. System Application Example



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## 7. Chip Block Diagram



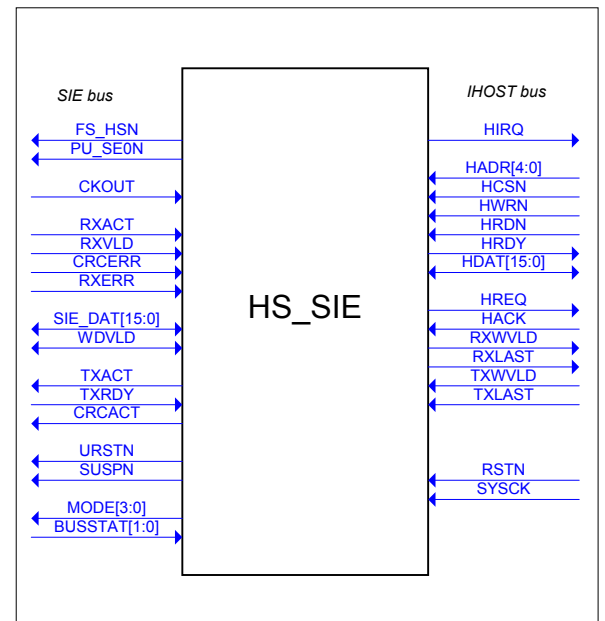
## 8. HS\_SIE IP Feature

### IP Feature

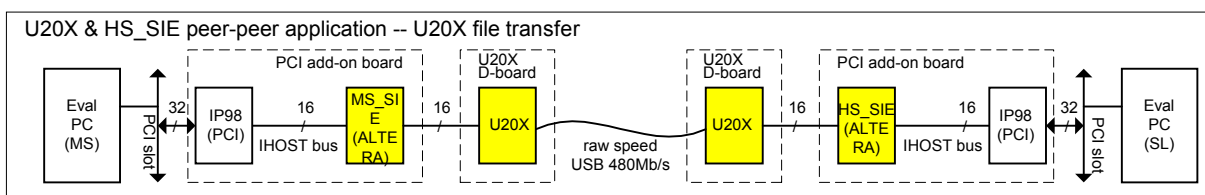
1. RTL design (easy to process migration)
2. Logic 15kgates, 1-p RAM 512Byte x 2, 64Byte x 1
3. Capable of HS chirp protocol and HS/FS judgement
4. Performs basic level USB operation  
such as token decode, miss-hit judge, RX error check, data toggle management, data buffering
5. Performs basic transaction flow control
6. Up to 5 endpoints supported
 

endpoint 0	R/W control tran	64bytes buffer
endpoint 1	W bulk out	512B (HS) / 64B (FS)
endpoint 2	R bulk in	512B (HS) / 64B (FS)
endpoint 3	W bulk out	8B (FS only)
endpoint 4	R bulk in	8B (FS only)
endpoint 5	R interrupt in	8B
7. IHOST IF  
general purpose 16bit bus (32bit expandable)  
register access (HCSN - HRDY handshake)  
DMA slave 1ch (HREQ - HACK handshake)  
IRQ 1ch

## 9. HS\_SIE Logical Pin out



## 10. Evaluation System Extension



## 11. Release Schedule

USB200	LSI sample	2001.1Q	HS_SIE	ALTERA ROM	2001.1Q
	evaluation board	2001.1Q		ASCP IP	2001.2Q
	MP	2001.1Q			
	ASCP IP	2001.2Q			

## 12. Contact

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