

# Kawasaki DisplayPort Receiver (KDP Rx) IP Information Sheet

Note: This brochure is a preliminary description for the products. Kawasaki Microelectronics Inc. and Kawasaki Microelectronics America, Inc. does not assure its functionality or feature and reserves the right to change them without notice.

## 1. General Description of DisplayPort IP

Kawasaki's DisplayPort receiver IP is compliant with the VESA's DisplayPort specification version 1.1a. The IP analyzes received DisplayPort data, and restructures video and audio data. TSMC 0.13um process is used. Here are the key features of the IP.

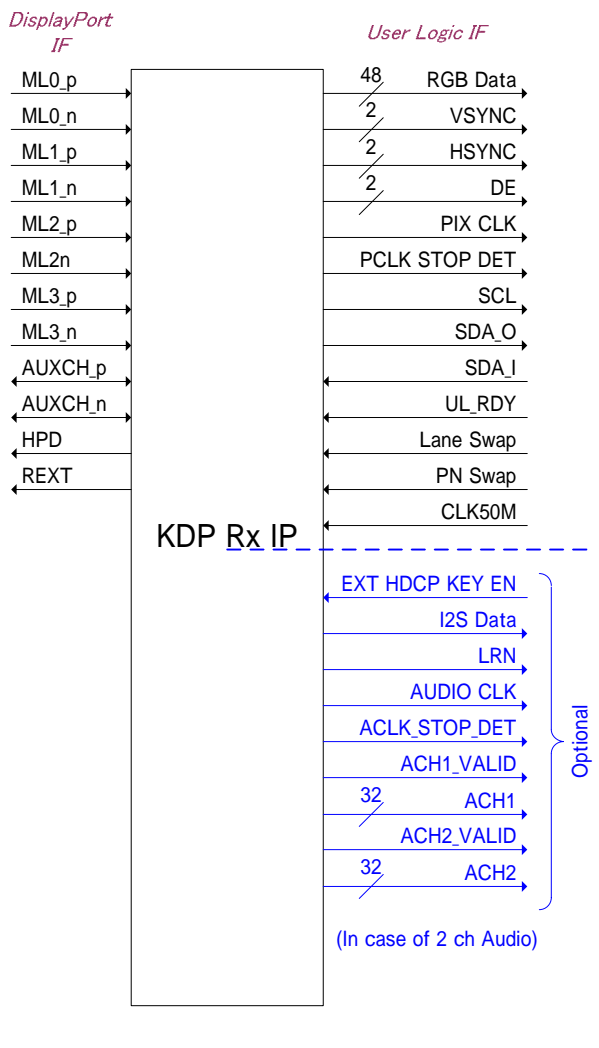
- Support both 2.7 Gbps and 1.62 Gbps
- 1.2V Analog Vdd to reduce power consumption
- No reference clock required
- Embedded 100 termination resistors
- Support adaptive equalizer
- Support Spread Spectrum Clocking
- Support 1 Lane, 2 Lane and 4 Lane configuration
- Lane swappable ( Lane 0 Lane 3 / Lane 1 Lane 2 )
- Positive and Negative of a differential pair swappable
- Support RGB444 mode and bit width of 6 and 8 bits
- Conventional video IF with Sync signals and pixel data
- Doubled Pixel bus width and 1/2 of original Pixel Clock Frequency output
- Optional I<sup>2</sup>S audio IF with 32, 44.1, 48, 88.2 and 96kHz sampling frequency
- Optional HDCP1.3 support with its HDCP key in embedded OTP

## 2. IP Feature

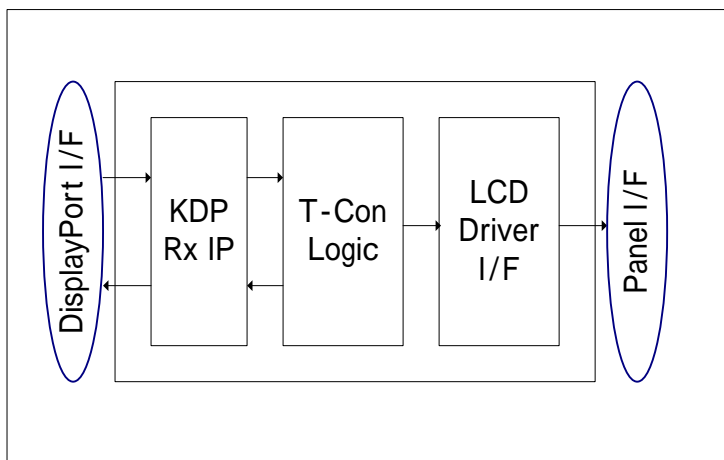
1. 0.13um standard cell technology (KS7500)
2. PMA implemented as hard macro
3. PCS and Link layer implemented as soft macro
4. Power Supply :
 

PMA	1.2V ± 0.1V
TTL I/O (HPD)	3.3V ± 0.3V, 2.5V ± 0.2V
Digital Core	1.2V ± 0.1V
5. Operational Junction Temperature : -40 - 125

## 3. Symbol



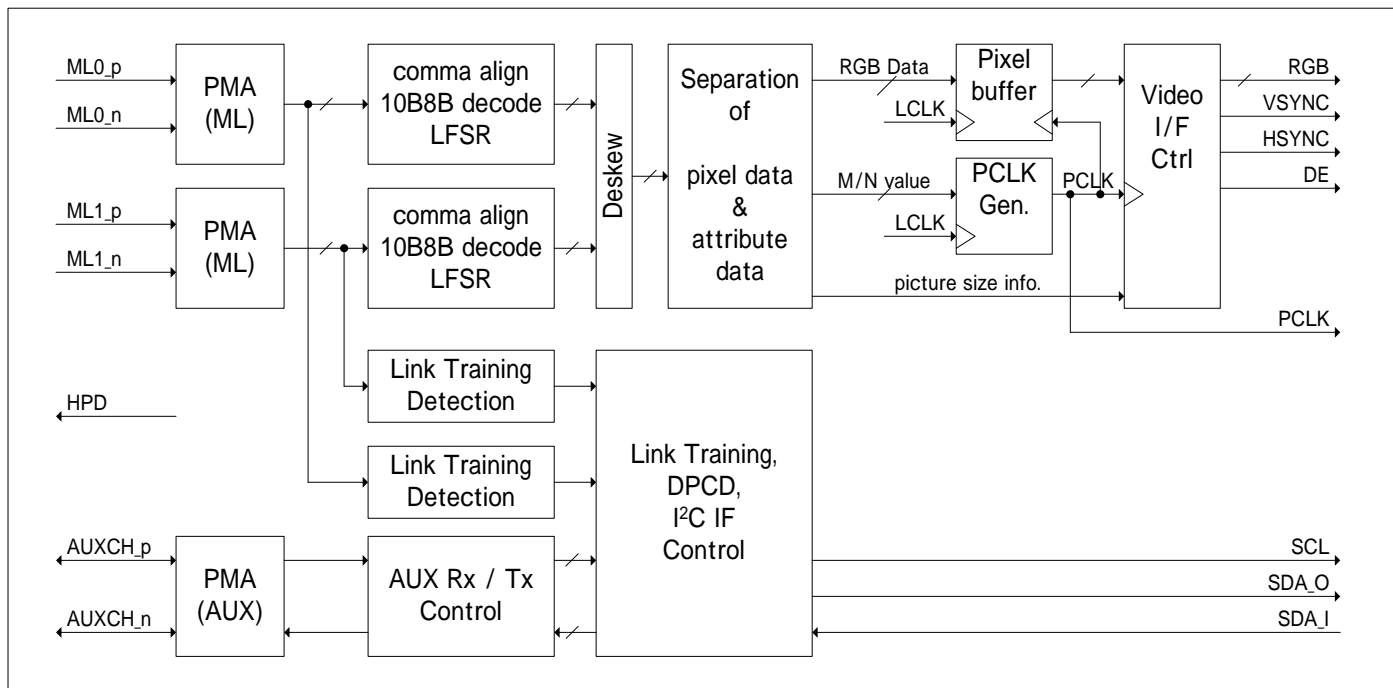
## 4. Application Example



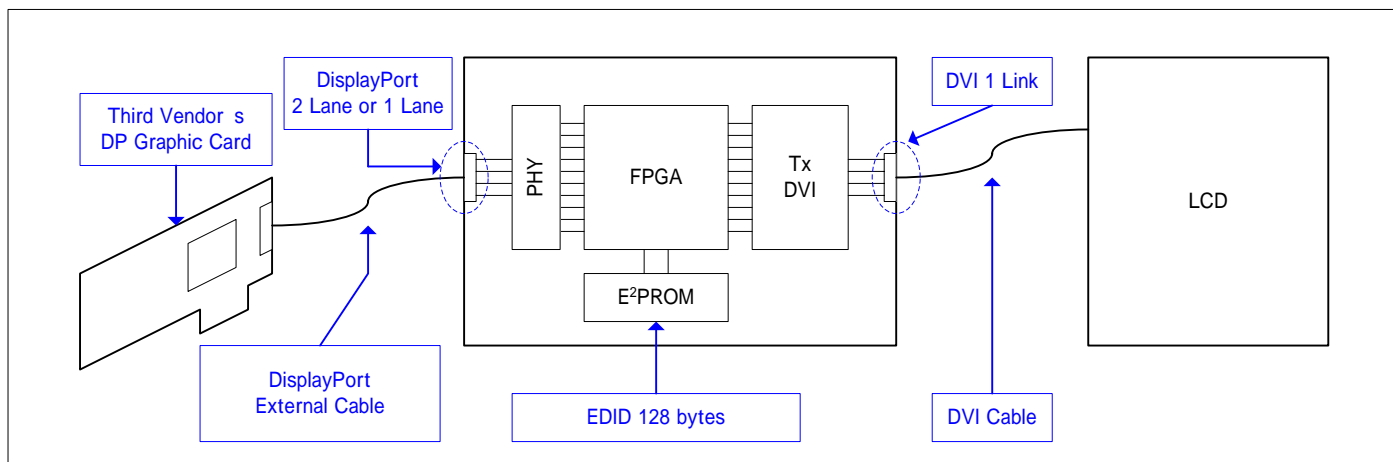
Kawasaki Microelectronics and Kawasaki Microelectronics America assume no responsibility or liability for (1) any errors or inaccuracies contained in the information herein and (2) the use of the information or a portion thereof in any application, including any claim for (a) copyright or patent infringement or (b) direct, indirect, special or consequential damages. There are no warranties extended or granted by this document. The information herein is subject to change without notice from Kawasaki Microelectronics and Kawasaki Microelectronics America.

# KAWASAKI MICROELECTRONICS, INC.

## 5. IP Internal Block Diagram ( case for 2 Lane )



## 6. Evaluation System Overview



## 8. Release Schedule

KDP IP	
FPGA Demo	Available
IP datasheet	Available
ASCP IP	Available

## 9. Contact

Japan:	Kawasaki Microelectronics, Inc. Sales Dept., Makuhari Techno-Garden B-11F, Nakase 1-3, Mihama-ku, Chiba, 261-8501, Japan Tel: +81-43-296-6131, Fax: +81-43-296-7419 URL : <a href="http://www.k-micro.com">http://www.k-micro.com</a>
Taiwan:	Kawasaki Microelectronics, Inc. Taiwan Branch RM.B 2F, Worldwide House, No.129, Min Sheng E.Rd., Sec3, Taipei 105, Taiwan, R.O.C. Tel: +886-2-2547-1297 Fax: +886-2-8770-6453 URL : <a href="http://www.k-micro.com">http://www.k-micro.com</a>
U.S.:	Kawasaki Microelectronics America, Inc., 2550 North First Street, Suite 500, San Jose, CA 95131 Tel: +1-408-570-0555, Fax: +1-408-570-0567 URL : <a href="http://www.k-micro.us">http://www.k-micro.us</a>

Kawasaki Microelectronics and Kawasaki Microelectronics America assume no responsibility or liability for (1) any errors or inaccuracies contained in the information herein and (2) the use of the information or a portion thereof in any application, including any claim for (a) copyright or patent infringement or (b) direct, indirect, special or consequential damages. There are no warranties extended or granted by this document. The information herein is subject to change without notice from Kawasaki Microelectronics and Kawasaki Microelectronics America.