

### FEATURES

- MIPS 32® 24Kf™w/L2C x 2 (AMP)
- 500MHz(466/433/400Mhz also selectable)
- 32kB L1 I/D cache
- 256kB L2 cache(0/128kB also selectable)
- Interconnect: Sonics MX® (XB/SL), Sonics3220™
- Memory Controller-400/533Mbps, Up to 4-rank on Eva-board (64bit/32bit selectable)
- GigE-MAC x 2 with Checksum engine
- IPSec/SSL accelerator
- Mixed grid-size/Library implementation
- CPU peripherals (16-channel Interrupt controller x 2, 8-channel Timer x 2, 16-channel GPIO, Watch Dog Timer x 2, UART)
- PCI-Express (End Point, 1Lane)
- 32kB Internal Memory
- 1-Ch DMA Controller
- I2C I/F for DDR configuration Serial-ROM access
- Power Control Unit to control dynamic/static power consumption
- USB (Device)
- External OCP I/F or PCIe-EP (PIPE)

### GENERAL DESCRIPTION

The CatsEye platform ASIC chip is part of an advanced SoC development system. The system enables advanced SoC designs to in a fraction of the time normally associated with complex development programs..

The CatsEye Development system includes all the functions needed to make a complete CPU subsystem for a variety of applications ranging from internet equipment such as routers and gateways, to entertainment devices such as media players and servers. The development system enables concurrent hardware and software designs providing the

ability to verify functionality before committing to the final ASIC chip. This approach results in a much shorter development time because all the core functions have already been developed, tested, and proven to interoperate together. Equally important is the reduced time to production since the software was developed and debugged concurrently with the hardware. The development systems' OCP interface offers the flexibility to add specific functionality to the design so each customer can add their own propriety IP to the chip and verify the functionality and full operation quickly.

### BLOCK DIAGRAM

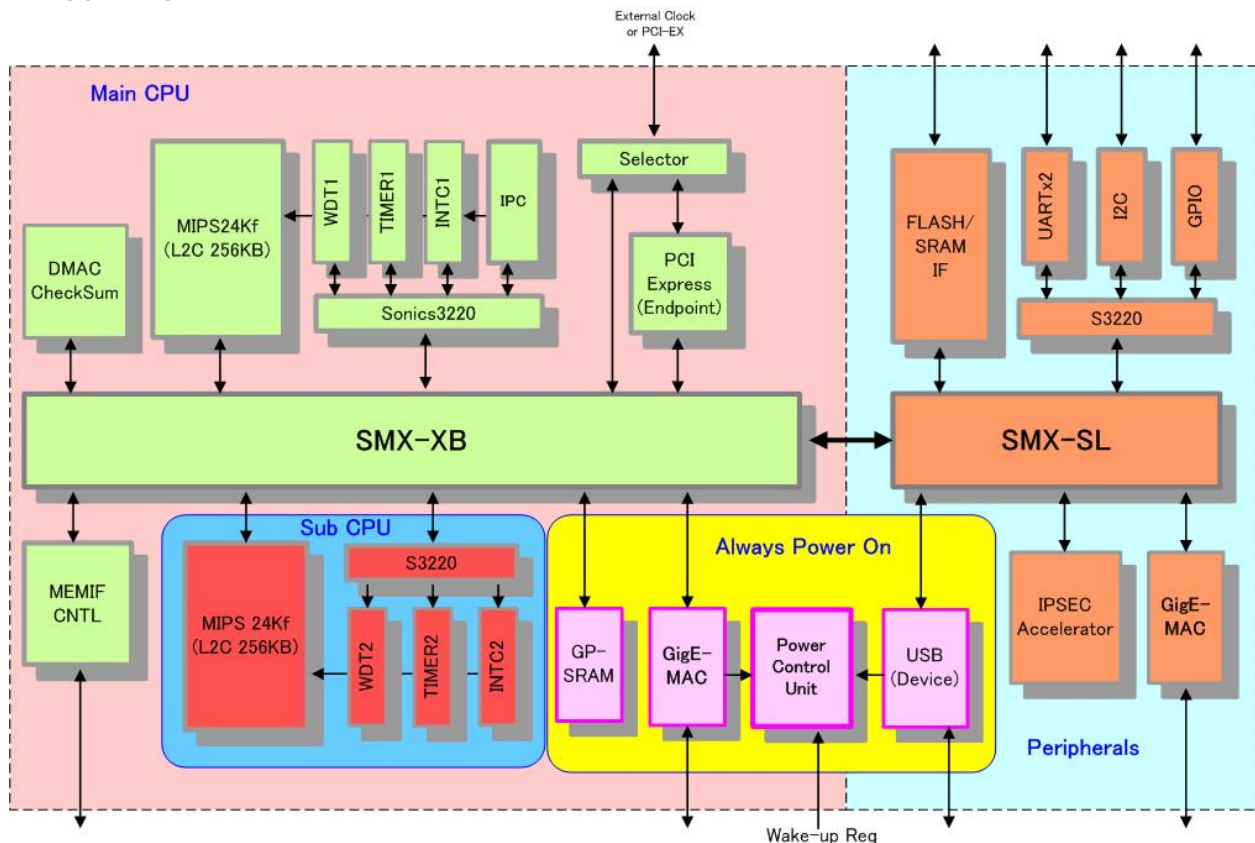


Figure 1 Functional Block Diagram

Fig1. Functional block diagram

**Reduced Development time:**

Compared to a conventional SoC development the CatsEye approach can cut the time to production by 6 to 12 months. The concurrent nature of design combined with the predefined base functionality enables the designer to focus on their specific function and IP.

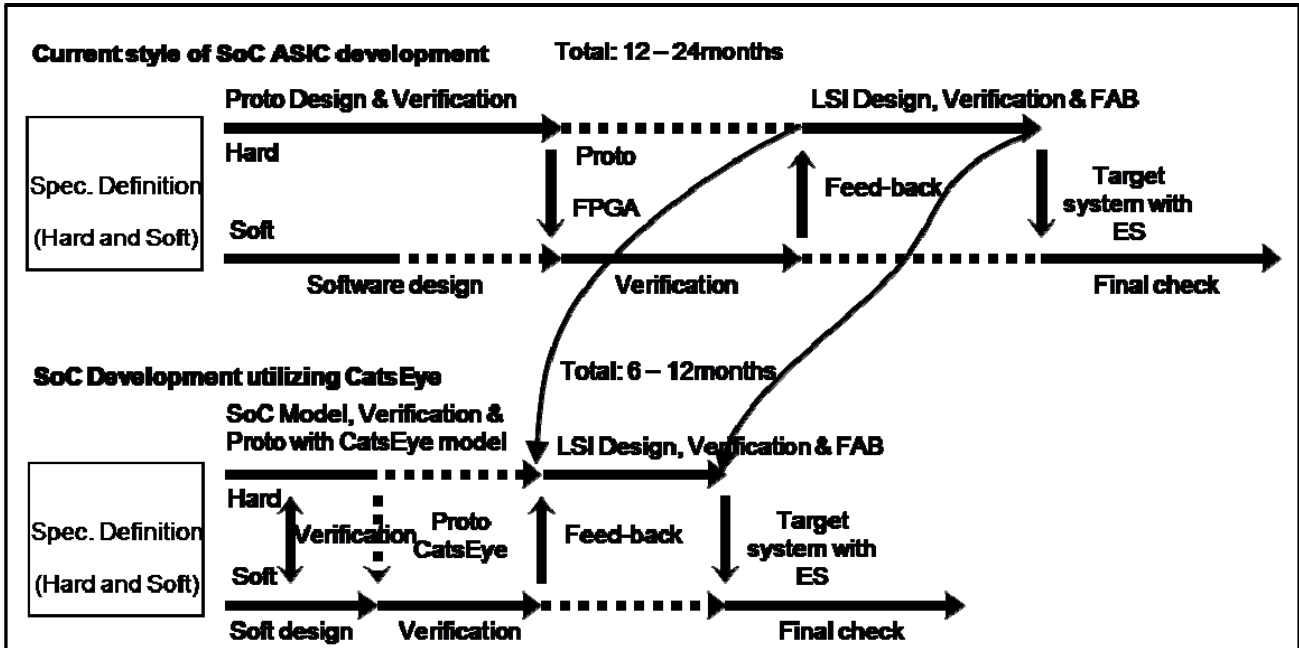


Figure 2 Time-line for SoC design

**Cost Effective:**

Once the basic functionality has been defined and verified the ASIC is developed with just the required IP and functionality, The final mass production chip contains only the IP and functionality needed.

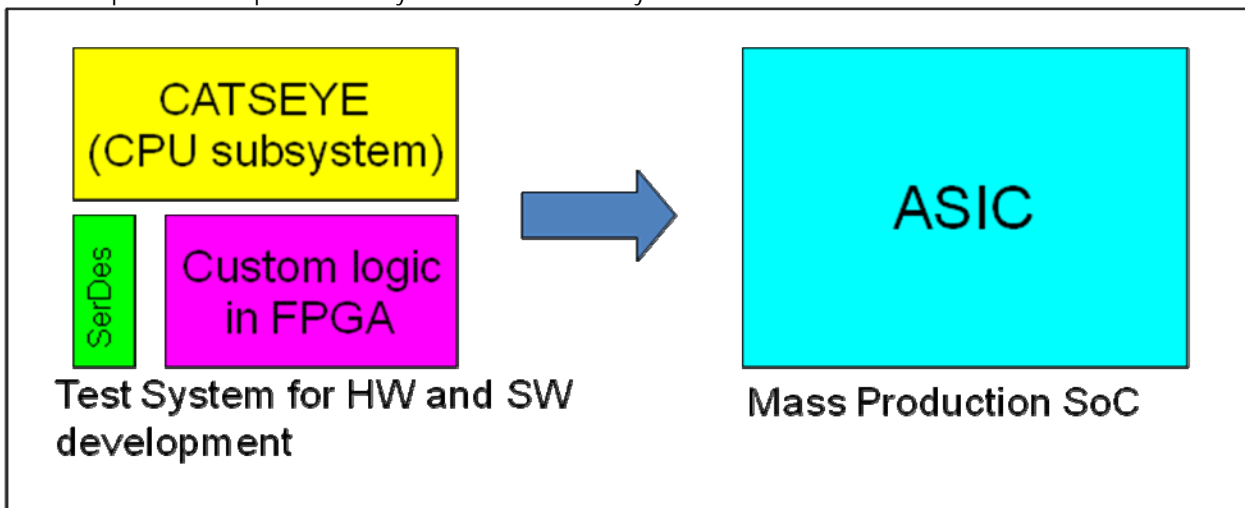


Figure 3 Mass Production ASIC

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